C1 cont'd

determining whether the timing constraint is satisfied; and

making a minimum change in the placing and routing when said delay gates are inserted.

C2

2. (Twice Amended) The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes placing a plurality of delay gates proximate to one another.

3. (Twice Amended) The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes placing a plurality of delay gates proximate to one another in the same clock line and in a region free of lines, other than clock lines, and free of gates, other than delay gates, so that clock lines are not influenced by other lines.

C3

4. (Thrice Amended) The method of designing a semiconductor circuit according to claim 2, wherein, in manually adjusting skew between clock trees, not deleting the first and last delay gates of a clock line.

C4

5. (Twice Amended) The method of designing a semiconductor circuit according to claim 3, wherein, in manually adjusting skew between clock trees, not deleting the first and last delay gates of a clock line.

IN THE ABSTRACT:

Replace the Abstract with:

C6

ABSTRACT OF THE DISCLOSURE

In a method of designing a semiconductor circuit having clock trees, a netlist is first generated. Then, delay gates are inserted into the netlist. Finally, inserted extra delay gates are deleted so that a timing constraint of the clock trees is satisfied. As a consequence, skew between the clock trees can be easily adjusted.